

ABSTRACT

In a conventional level conversion circuit, the variation of output signals from a low level to a high level is slower than that from a high level to a low level. As a consequence, on the part of a circuit receiving signals from such a level conversion circuit, signals have to be accepted at the later signal timing, resulting in the problems of more complex timing design and of a longer time taken by signal transmission, which impedes raising the system speed. The configuration is such that a level conversion circuit is composed of a level shift circuit for supplying a level-converted signal in the same phase as the input signal and a signal in the reverse phase thereto and a follow-up circuit responsive to the earlier of the output signals of the level shift circuit for generating an output signal, wherein the follow-up circuit consists of an inverter circuit in which two p-channel type MOS transistors and two n-channel type MOS transistors are connected in series between a first voltage terminal and a second voltage terminal, of which one pair is used as input transistors and the remaining pair of transistors are subjected to feedback based on the output signal of the level shift circuit to be quickly responsive to the next variation.

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